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Patents Claiming a Range of Values, Such as Gate Sizes for Semiconductor Chips, Must Enable One of Ordinary Skill to Make and Use the Entire Claimed Range

Jul 6, 2020

Reading Time : **4 min**

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In December 2018, complainant Tela Innovations, Inc. filed a complaint in the ITC against various semiconductor companies, including Acer, Asus Computer, Intel, Lenovo and Micro-Star ("Respondents") for importing products that infringe five of Tela's patents that relate to semiconductor chips with gate structures. On May 22, 2020, after an evidentiary hearing, Administrative Law Judge (ALJ) Cameron Elliot issued an initial determination, finding that claims of U.S. Patent No. 10,141,334 ("the '334 Patent") were not enabled because they required undue experimentation to manufacture chips at the low end of the claimed size ranges.

Under 35 U.S.C. § 112(a), or pre-AIA § 112, ¶ 1, a valid patent must describe "the manner and process of making and using" the claimed invention. A claim is adequately enabled when the specification teaches "those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation." The Federal Circuit has articulated a set of factors to consider in assessing enablement, including: (1) the quantity of experimentation necessary; (2) the amount of direction or guidance presented; (3) the presence or absence of working examples; (4) the nature of the invention; (5) the state of the prior art; (6) the relative skill of those in the art; (7) the predictability or unpredictability of the art; and (8) the breadth of the claims. *In re Wands*, 585 F.2d 731, 737 (Fed. Cir. 1988).

The ALJ began with claim construction to determine the "full scope" of the claims. The claims recite ranges of gate pitch and width—sizing features of semiconductor chips—and specifically, "a gate pitch of less than or equal to about 193 nanometers" and "a width of less than or equal to about 45 nanometers." The Respondents indicated, however, that there was a

"(yet unknown) physical limit to how small gate widths and pitches can ultimately be." According to the ALJ, the parties agreed that a "gate pitch" should be construed to range from about 40 to 193 nanometers. With respect to "gate width," however, the parties did not agree on a lower bound. Because Tela's expert, Dr. Hook, testified that seven nanometers was within the scope of the claimed range, and the parties agreed that his testimony was authoritative on the knowledge of one of ordinary skill, the ALJ construed "gate width" to range from about 7 to 45 nanometers.

The ALJ then applied the *Wands* factors to determine whether the full scope of the claimed ranges were enabled for a person of ordinary skill in the art (POSITA). To start, the ALJ looked to the related factors (1), the quantity of experimentation necessary, and (6), the relative skill of those in the art. Dr. Hook testified that a seven nanometer node was "beyond today's manufacturing" abilities and that, to reduce the scale of integrated circuit chips in a single process node, it takes "the full-time effort of at least 1,000 engineers, 95% of whom have doctorates, and 'billions' of dollars in research and development expenses." Although such labors are "commonplace" and "business as usual" in the semiconductor industry, the ALJ found that "they are surely far from 'routine' within the meaning of *Wands*" and "clearly well beyond the capabilities of a POSITA."

Turning to factor (2), the ALJ weighed the amount of direction or guidance presented. The ALJ noted the '334 Patent is "silent on the process" of resolving the technological hurdles to scale down chip size. The patent's disclosure of the standard "CMOS" semiconductor fabrication process provided no guidance to a skilled artisan on how to shrink a chip's size. According to the ALJ, the specification presupposes that any technological hurdles to shrinking gate width and pitch will be overcome with time, and "leaves entirely to someone else the task of solving the problems preventing a skilled artisan from practicing the full scope of the invention."

Factors (3), the presence or absence of working examples, and (5), the state of the prior art, also weighed in favor of finding undue experimentation. The working examples in the '334 Patent did not pertain to the lower bounds of the claimed ranges, and expert testimony confirmed that working examples of the lower bounds of the claimed ranges did not exist. Factor (4), the nature of the invention, however, weighed slightly against a finding of undue experimentation. The ALJ noted that the claimed ranges are not the "heart of the invention," which is "the combination of various chip layers possessing rectilinear features" as opposed to the size of those features.

Next, the ALJ determined that factor (7), predictability of the art, weighs against undue experimentation based on the concept of Moore's Law, which provides that integrated circuits halve in area on average once every two years. Finally, factor (8), the breadth of the claims, weighed against a finding of enablement because they included gate width and pitch ranges with lower bounds beyond what could be made and used at the time of the invention and even at the time of the decision.

Having weighed the *Wands* factors, the ALJ held that the breadth of enablement in the patent specification is not commensurate in scope with the claims. Consequently, the '334 Patent was found invalid for lack of enablement.

Practice tip: Patent owners should be particularly careful when drafting claims directed to ranges, ensuring that the patent specification enables the full scope of the claimed range. This applies to open-ended ranges with no upper bound, but also, as seen in this investigation, ranges that extend to zero. A POSITA must be able to make and use the full scope of any claimed range at the time of the invention.

Certain Integrated Circuits & Prods. Containing Same, Inv. No. 337-TA-1148 (U.S.I.T.C. May 22, 2020) (ALJ Elliot)

Categories

International Trade Commission | 35 U.S.C § 112 ¶ 6

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